The Design-Manufacturing Roadmap

Technical Session 1

The Deep Submicron Hell of Physical Design Keynote

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Abstract

Designers, EDA vendors, and semiconductor manufacturing equipment vendors have fundamentally conflicting goals, with each community engaged in incremental, linear extrapolation of its current trajectory. To maintain the cost (i.e., value) trajectory of Moore's Law requires the cooperation and co-evolution of these communities. From the EDA perspective, focus areas include .

- direct, manufacturability-driven optimization of cost and value;
- restricted and/or error-tolerant design;
- intelligent data preparation;
- "analog rules" (as opposed to "digital", 0/1 rules);
- and a host of other potential layout and design optimizations.

The basic need is for a "bidirectional design-manufacturing data pipe", driven by cost and value. Design functional intent must be passed to manufacturing, so that incremental manufacturing resources directly improve circuit performance, parametric yield, and/or other measures of product value. Going the other way, models of manufacturing equipment and processes must be passed up to design, so that, e.g., only manufacturable and verifiable layouts will be created. This talk addresses key design challenges for mask, litho and cost-driven product development - as well as a roadmap for design-manufacturing integration.

Curriculum Vitae

Andrew B. Kahng is professor in the UC San Diego CSE and ECE departments. He was the founding General Chair of the International Symposium on Physical Design and co-founded the Workshop on System-Level Interconnect Planning. Since 2001, he has chaired the U.S. and international working groups for Design Technology for the International Technology Roadmap for Semiconductors. His research is on physical design and performance analysis of VLSI, as well as the VLSI design-manufacturing interface. In the latter area, results span optimal phase conflict resolution, dummy fill syntheses, min-cost lithographic correction, subfield scheduling for mask write, and generation of compressible layouts.