Efficient RISC-V Processor Verification via Cross-Level Testing

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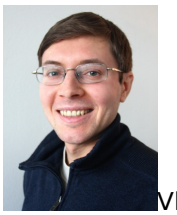
Abstract

We present an efficient cross-level testing approach for processor verification targeting the RISC-V Instruction Set Architecture (ISA). It works by generating an endless instruction stream without restrictions on the generated instructions by evolving the instruction stream on-the-fly during simulation. An Instruction Set Simulator (ISS) is leveraged as reference model for the RTL core under test in a tightly coupled cross-level co-simulation setting. This enables a very efficient and comprehensive testing process. As a case-study we present first results on the verification of the 32 bit pipelined RISC-V core of MINRES The Good Folk (TGF) Series (the ecosystem core of the BMBF funded Scale4Edge project). Our approach has been very effective in finding several serious bugs.

Biography



Vladimir Herdt received the M.Sc. degree in computer science from the University of Bremen, Germany, in 2014. Afterwards, he started as a PhD student with the Group of Computer Architecture. In 2020, he received the Dr.-Ing. degree in computer science. Since 2020, he is Senior Researcher at the German Research Center for Artificial Intelligence (DFKI) and University of Bremen. His current research interests include virtual prototyping as well as verification and analysis techniques with a particular focus on RISC-V. In these areas he published more than 30 peer-reviewed journal and conference papers with a Best Paper Award at the FDL. He is recipient of the Springer BestMasters award.