Nanometer-Era Design for Manufacturability

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Abstract

In the nanometer era, the spectrum of physical phenomena that can contribute to significant yield losses is mind-boggling. The most accurate way of accounting for these effects is to provide accurate physical models and then simulate the actual IC layout to estimate the impact on yield and performance. Such a simulator must be calibrated to the actual manufacturing process by specially designed test structures that cover all possible layout patterns found in real products. A set of Characterization Vehicles (CV™) that are used for extraction of defectivity, fail rates and performance variability characteristics of a given fabrication process will be presented. This modeling-based approach can be then used for generation of “guaranteed to yield” IP blocks and can also serve as a yield sign-off tool for the entire IC layout. Examples of the improved set of IPs and silicon verification results demonstrating the yield gain will be shown. Then a rigorous decision tree based approach to the root cause analysis and fixing of the top yield detractors will be introduced, followed by a comprehensive set of product engineering solutions. Finally the talk covers the actual yield learning results obtained by employing this comprehensive methodology to the process and product ramps for several lead products in the most advanced technology nodes.

Curriculum Vitae

Andrzej J. Strojwas has served as a technical advisor to PDF since the company was launched and was appointed PDF’s Chief Technologist in 1997. Currently the Keithley Professor of Electrical and Computer Engineering at Carnegie Mellon University, Dr. Strojwas’ career spans over 25 years as an expert in the electronics manufacturing industry. He has held senior technical positions at Harris Semiconductor Co., AT&T Bell Laboratories, Texas Instruments, NEC, Hitachi, SEMATECH and KLA-Tencor, and has consulted for several semiconductor companies, equipment vendors and EDA companies in the area of statistically based CAD/CIM of VLSI circuits. Dr. Strojwas is an IEEE Fellow.