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Sigma65: Technologybased Modeling and Analyzing Methods considering variation in the 65nm node

$\sigma 65$

The topic of the investigations planned over the next years will be the introduction and full deployment of next generation technologies in digital IC design. This includes for instance the 65-nm node. Resulting from decreasing structures, new relations between the components of a chip and its environment have to be taken into consideration. The growing level of uncertainties of key parameters within a chip and between different chips in the sub-100 nm area plays a more and more important role. The process spreads have to be consequently considered in the design process. The project especially takes the description levels into account that are closely related to the process technologies. During the project period, procedures and methods will be developed that allow to determine probability distributions of parameters that describe circuits at a higher level of abstraction (gate or block level) based on the distributions of the process and transistor level parameters. The high level models shall directly depend on the main technology uncertainties as accurate as necessary.

Project coordination:

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Project partners:

- [Fraunhofer Institut für Integrierte Schaltungen \(IIS\)](#)
- [Infineon Technologies AG](#)
- [MunEDA GmbH](#)

Research partners:

- [Leibniz Universität Hannover](#)
- [Technische Universität München](#)

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<http://sigma65.eas.iis.fraunhofer.de>

Project Information

Final Report

NL 04 2009 (PSB)

NL 04 2008 (PB)

NL 02 2008 (PKB)

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Used Abbreviations

Abbreviation	Meaning
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PR Project Report
SPR Short Project Report
PN Project News
FPR Final Project Report

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