Setting up a debug solution with Lauterbach Debug Hardware and Software for a custom implementation of a RISC-V core - Lessons Learned

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Abstract

In order to enable efficient software and firmware development for a RISC-V core with custom instructions, full-featured SW debug capabilities are mandatory. This implies not only a customized hardware implementation of an on-chip debug system (OCDS), but also an aligned debugging software stack. In particular, the integration of hardware and software is essential for a complete debug solution. In this talk, we will present first the initial setup with open-source GNU GDB, OpenOCD, and J-Link. This initial setup is sufficient for proof of concept and deepening our understanding on the specification. However, open-source components are often not up-to-date and lack support. For commercial use, we migrated our debug infrastructure towards the Lauterbach solution, which includes TRACE32, Power Debug Pro, and debug cable. In this contribution, we would like to elaborate on our activities and share the lessons we learned when moving from an open source to a commercial solution for SW debug.

Biography

 Mr. Zhao Han received his B.Sc. degree in 2013 from the China University of Mining and Technology, China and M.Sc. degree in 2018 from the University of Erlangen–Nuremberg, Germany with specialization in information and communication technology. Mr. Han is currently working as System Engineer Adviser at Infineon Technologies AG, Germany.