Workshop “Chip Design for SME: Chances und Hurdles!“

The importance of microelectronics for the European industry is currently in the spotlight even more than before – the "chip crisis", especially in the automotive sector, has been a front-page topic for quite some time.

The EU Commission and national governments are preparing a variety of initiatives to coun-teract this. The EU Chips Act with a volume of EUR 43 billion provides the framework. The location of new manufacturing capacities in Europe dominates the headlines, but the sus-tainable strengthening of the design capability for ASICs ("chip design") in Europe is also identified as a central topic. This design capability is to be sustainably improved with various initiatives.

How can SMEs benefit from this? Is chip design only relevant for global corporations, or can chip design also help SMEs to improve their market position?

The edacentrum and its technical advisory board are convinced that this question is of central importance for the future of European industry, which is driven by medium-sized "hidden champions". It is essential to design the necessary initiatives now to make access to ASIC design more commonplace for SMEs as well.

In order to achieve this goal, we want to propose suitable measures to the national funding agencies and other stakeholders and are organising a target-oriented

Workshop “Chip Design for SMEs: Chances and Hurdles!“

on June 28th, 2022, 1.30 - 5 pm, in Dresden, Germany

Location: Fraunhofer IIS EAS, Münchner Str. 16,01187 Dresden, Raum A0.02

In this workshop we want to address the following topics:

- Do SMEs see a benefit in developing or having developed their own ASICs?
- What obstacles currently prevent SMEs from putting this into practice?
- What role does the (possibly lacking) availability of experts play?
- What concrete approaches can be used to address the specific needs of SMEs?
- How can an ecosystem be established, especially for SMEs, that makes chip design much more accessible than before by providing essential components such as IP blocks, EDA tools and design flows based on them, as well as access to manufacturers through process design kits?

In the workshop, concrete recommendations for action will be developed, in particular also on the topic of the shortage of skilled workers.

We therefore invite interested parties to present their own experiences and requirements in the workshop:

- Successful approaches to ASIC design ("Success Stories in Chip Design").
- Obstacles to designing your own ASICs
- Topics to be addressed across companies (training of skilled workers, research policy, etc.)

Are you interested in participating? We look forward to hearing from you! Please contact us.

The workshop is offered free of charge. It will be held in English.

This focused workshop to develop recommendations for action will take place in the run-up to the ADTC and edaWorkshop22 event [1] to which we also cordially invite you.

Best regards

Prof. Dr. U. Schlichtmann
Chair of ADTC &
edaWorkshop and
Vice Chairman edacentrum

Prof. Dr. W. Nebel
Chair edaWorkshop and
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