Breaking Down the Manufacturing Design Firewall - DFM Flows are Becoming Reality

Technical Session I

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Abstract

Since the early days of wafer processing the separation of design and fabrication has worked impressively well for many generations of technology. At 130nm and below, however, many physical effects have begun to strain this ability, leading to a gap between design and silicon performance. If this gap becomes too large, it becomes impossible to manufacture a design at high yield due to systematic and random factors. Mixed signal and analog designs in smaller geometries put additional DFM requirements.

To reduce the design-manufacturing gap, three options exist: 1. to improve the models; 2. to modify the manufacturing process; and 3. to improve both. The first solution (DFM in the traditional sense) encompasses additional tools and methodologies that are introduced in the design flow and the post processing of the GDSII layout database prior to mask manufacturing. The second solution focuses on tools and methodologies introduced in manufacturing to mitigate factors influencing parametric yield (called "Manufacturing for Design" or MFD).

This talk will review the current status of DFM and MFD efforts in the semiconductor and EDA industry and will especially discuss the DFM requirements for analog and mixed signal designs.

Biography

 **Wolfgang Fichtner Senior Vice President and General Manager Silicon Engineering GroupSynopsys, Inc.**

Wolfgang Fichtner received the M.S. degree in physics and the Ph.D. degree in electrical engineering from the Technical University of Vienna, Austria, in 1974 and 1978, respectively. From 1979 through 1985, he worked at AT&T Bell Laboratories, Murray Hill, NJ. He was Professor and Head of the Integrated Systems Laboratory at the Swiss Federal Institute of Technology (ETH) from 1985 to 2004.

In 1993, he founded ISE Integrated Systems Engineering AG, a company in the field of TCAD. In November 2004, he joined Synopsys Inc, Mountain View, CA, as Vice President and General Manager of the TCAD Business Unit. He is currently Senior Vice President and General Manager of the Silicon Engineering Group at Synopsys. In 2000, he received the IEEE Andrew S. Grove Field Award for his contributions to TCAD. In the areas of integrated circuit design, Technology CAD and solid state physics, he has published more than 450 papers.