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# **Design Enablement for 90 nm and Beyond - The New Paradigm in the Semiconductor Industry**

## **edaForum05 Presentation**

### **Business Session II**

**Anton Ossner**

## **Chartered Semiconductor Design Enablement for 90 nm and Beyond The New Paradigm in the Semiconductor Industry**

### **Abstract**

Beginning at 90 nm, the high level of system integration on a single chip, process density and the complex interaction between design and process are shaping a new semiconductor industry landscape. The traditional model of buying best-in-class solutions from the value chain to enable functional designs no longer works. Broader, earlier and deeper levels of collaboration across the value-chain are required to incorporate system-level design needs in silicon. This re-aggregation of efforts, in turn, is driving the value-chain toward jointly developing and building solutions.

The presentation will detail the business model and elements of the industry's first common design enablement platform for 90 nm and beyond. Championed by Chartered Semiconductor Manufacturing and IBM, the initiative has garnered strong support and participation from system leaders, such as Samsung Electronics, and leading EDA and IP companies. The topic will also cover how early adopters can optimize complex SoC designs in silicon and develop compatible GDSII files to enhance design portability and multi-sourcing flexibility.

### **Biography:**



**Anton Ossner Director Business Development Europe Chartered Semiconductor Europe Ltd.**

He joined Chartered in January 2001 and is responsible for Business Development within the Company's Europe region. He is based in the Munich office of Chartered.

He has 16 years of experience in the semiconductor industry. Prior to joining Chartered, he has held several management positions related to Design Systems and Design Methodology at the Central Design Automation Department as well as the SmartCard Business Division at Infineon Technologies AG in Munich. Previously he was working at LSI Logic Europe and had responsibility for the Design Tools and Methodology Support of all Customers of LSI Logic and its Design Centers in Europe. He holds a degree in semiconductor electronics from Technical University of Munich, Germany.

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