Energy Efficient RISC-V Implementations in 22 nm

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Abstract

An overview of research projects at HPSN using RISC-V processors is presented. We explain our motivations to use RISC-V and the RI5CY micro-architecture for our processing elements. The integration of the CPU and the scalability of the PE architecture is demonstrated with two example projects. A comparison shows that our chip implementations in 22 nm FDSOI technology reach state-of-the-art energy efficiency numbers.

Biography

Heiner Bauer received his diploma degree in Electrical Engineering from TU Dresden in 2017. Currently he is a research assistant with the Chair of Highly-Parallel VLSI Systems and Neuromorphic Circuits (HPSN) at TU Dresden. His research interests include microprocessor architecture, low-power design, and reconfigurable computing.