RISC-V Trainings

5th Workshop on RISC-V Activities

7 November 2022

This joint academic/industry workshop aims to stimulate the exchange of information among the attendees about already existing or planned RISC-V activities. The workshop provides a platform for how these activities can be extended across projects or to develop new ideas, activities and collaborations. This workshop has been initiated by the BMBF funded project Scale4Edge [1] and will be executed in conjunction with the edaForum22 and MICROELECTRONICS FOR FUTURE 22 [2].

Date: 7 November 2022

Location: Hotel NH Collection Berlin Mitte, Friedrichstraße 96, 10117 Berlin, Germany [3]; in Google Maps [4]

Workshop language: English

RISC-V is one of the hottest trends in the industry these days, with its mature software toolchain and many hardware processor providers offering implementations ranging from textbook open-source cores to high-end commercial ones. The freedom to configure and customize the RISC-V ISA in accordance to the system needs, including custom instructions, is one of its strongest appeals, making custom RISC-V CPUs an attractive choice for an unprecedented number of companies. However, the challenge of actually designing a RISC-V core with custom extensions and ensuring its correct functional behaviour is still significant, even more in environments with high safety and security expectations.

About the Workshop series: https://www.edacentrum.de/en/risc-v/trainings [5]

Program: https://www.edacentrum.de/en/events/risc-v/2022/program [6]

Registration

- Registration deadline: 31 October 2022 AoE*)
  Registration is open!
  Registrations can be done online at https://www.edacentrum.de/en/risc-v/registration [7] only!

Deadlines

Short abstract deadline:	Sep 28, 2022 AoE*)

Author notification:	Oct 7, 2022 AoE*)
Program available:	Oct 14, 2022 AoE*)
Registration deadline:	Oct 31, 2022 AoE*)

*) AoE = Anywhere on Earth

Organizing Committee

- Oliver Bringmann, Universität Tübingen, DE
- Wolfgang Ecker, Infineon Technologies, DE
- Andreas Mauderer, Robert Bosch GmbH, DE
- Daniel Müller-Gritschneder, Technische Universität München, DE
- Wolfgang Müller, Universität Paderborn, DE
- Dieter Treytnar, edacentrum, DE
- Andreas Vörg, edacentrum, DE
- Stefan Wallentowitz, Hochschule München, DE

In case of questions, please contact:
Andreas Vörg or Dieter Treytnar
risc-v@edacentrum [dot] de

Previous editions of the Workshop on RISC-V Activities

4th Workshop on RISC-V Activities

2 December 2021

This joint academic/industry workshop aims to stimulate the exchange of information among the attendees about already existing or planned RISC-V activities. The workshop provides a platform for how these activities can be extended across projects or to develop new ideas, activities and collaborations. This workshop has been initiated by the BMBF funded projects SAFE4I [8] and Scale4Edge [1] and will be executed in conjunction with the edaWorkshop21.

Date: 2 December 2021 9:30-17:35 CET

Location: Online with Microsoft Teams

Workshop language: English

Program

The full program is available at https://www.edacentrum.de/en/events/risc-v/2021/program [9]

Registration

Registrations can be done online at https://www.edacentrum.de/en/risc-v/registration [7] only!
Registrations are possible until 25 November 2021 AoE*)

*) AoE = Anywhere on Earth

We will have two invited keynote talks for the topic "T**owards Trustworthy RISC-V Processors for Safety-critical Applications**"

RISC-V is one of the hottest trends in the industry these days, with its mature software toolchain and many hardware processor providers offering implementations ranging from textbook open-source cores to high-end commercial ones. The freedom to configure and customize the RISC-V ISA in accordance to the system needs, including custom instructions, is one of its strongest appeals, making custom RISC-V CPUs an attractive choice for an unprecedented number of companies. However, the challenge of actually designing a RISC-V core with custom extensions and ensuring its correct functional behaviour is still significant, even more in environments with high safety and security expectations. In this session, we present an automated flow to generate RISC-V cores with custom extensions together with their complete verification.

Keynote:
Talk 1: Towards Trustworthy RISC-V Processors for Safety-critical Applications

 **Eyck Jentzsch (MINRES Technologies, D)**
Biography: Eyck Jentzsch holds a Dipl.-Ing. from the Technical University Ilmenau and has more than 25 years experience in microelectronics and semiconductor design. He is working at MINRES as General Manager and focuses on virtual platform modelling, development, and application as well as RISC-V IP development and verification. Prior to that he worked at Cadence Design Systems Inc. And Siemens in various full- and semi-custom as well as system level design and verification positions.

Keynote:
Talk 2: Towards Trustworthy RISC-V Processors for Safety-critical Applications

 **Salaheddin Hetalani (Siemens EDA, D)**
Biography: Salaheddin Hetalani holds a M. Sc. in Embedded Computing Systems as a joint degree from the Technical University of Kaiserslautern and Southampton University and has around 3-year experience in formal design verification. He is working at Siemens EDA as Field Application Engineer and focuses on application and development of RISC-V and bus protocol VIPs

And we will have a panel session on

The RISC-V Software Ecosystem: Where we are and where are we going?
Moderator: Stefan Wallentowitz (Munich University of Applied Sciences, D)

Considering the youth of RISC-V, the instruction set architecture has an advanced software ecosystem. With the ever-increasing number of ratified instruction set extensions and the emergence of a variety of hardware platforms, the software ecosystem is constantly in flow and several groups work on solidifying the software ecosystem, filling gaps and improving performance. In this panel discussion we will first get an overview of the state of the software ecosystem by Mark Himelstein (CTO of RISC-V) and Philipp Tomisch (Head of RISC-V Software Task Group). After that we will discuss the RISC-V software ecosystem and where it is heading. We are seeking your questions and suggestions during the panel, and you can also send it in advance to stefan [dot] wallentowitz@hm [dot] edu.

Panelists
Ingo Feldner (Bosch, D)
Drew Fustini (Beagleboard, US)
Mark Himelstein (RISC-V International, CH)
Philipp Tomisch (TU Vienna and VRULL GmbH, AT)

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- Stefan Wallentowitz, Hochschule München, DE

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Information about the organizing projects

- SAFE4I website: https://www.edacentrum.de/projekte/SAFE4I [8]
- Scale4Edge website: https://www.edacentrum.de/projekte/Scale4Edge [10]

3rd Workshop on RISC-V Activities

Virtual Online Event, 8 October 2020

This joint academic/industry workshop aims to stimulate the exchange of information among the attendees about already existing or planned RISC-V activities. The workshop provides a platform for how these activities can be extended across projects or to develop new ideas, activities and collaborations. This workshop has been initiated by the BMBF funded projects COMPACT, SAFE4I and Scale4Edge.

Location: Virtual Online Event

Workshop language: English

Deadlines

- Registration deadline: Oct 7, 2020
- 3rd Workshop on RISC-V Activities: Oct 8, 2020 9:00-17:00

3rd Workshop on RISC-V Activities: https://www.edacentrum.de/en/risc-v [11]

Program: **The program of the workshop is available at https://www.edacentrum.de/en/events/risc-v/2020/program [12] .**

Invited Talks:

- **Wolfgang Ecker (Infineon Technologies, DE)** on "RISC-V Scale4Edge Ecosystem - Motivation and Objectives" [13]
- **Jeremy Bennett (Embecosm, UK)** on "RISC-V Software Ecosystem" [14]
- **Zvonimir Bandić (Western Digital, US)** on "CHIPS Alliance and Western Digital's RISC-V Related Activities" [15]
- **Calista Redmond (RISC-V Foundation International, US)** on "Collaboration and adoption Accelerate with RISC-V International with Live Q&A" [16]

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- Wolfgang Müller, Universität Paderborn, DE
- Dieter Treytnar, edacentrum, DE
- Andreas Vörg, edacentrum, DE
- Stefan Wallentowitz, Hochschule München, DE

Information about the organizing projects

- COMPACT website: https://www.edacentrum.de/projekte/COMPACT [17]
- SAFE4I website: https://www.edacentrum.de/projekte/SAFE4I [8]
- Scale4Edge website: https://www.edacentrum.de/projekte/Scale4Edge [10]

2nd International Workshop on RISC-V Research Activities

Technical University Munich (TUM), Germany, 28 February 2019

This joint academic/industry workshop aims to stimulate the exchange of information among the attendees about already existing or planned RISC-V research activities. The workshop provides a platform for how these activities can be extended across projects or to develop new ideas, activities and collaborations. This workshop has been initiated by the German BMBF funded projects COMPACT, CONFIRM and SAFE4I.

Location: TU Munich, Arcisstr. 21, 80333 Munich, Buildung 9, 2nd floor, ROOM 4905

Workshop language: English

Registration fee: 70 € plus VAT

Program:

The program of the workshop is available at https://www.edacentrum.de/en/events/risc-v/2019/program [18] .

There is an optional Come-Together/Dinner at the “Schneider Bräuhaus! ” on the evening before the workshop.

Deadlines:

- Registration deadline: Feb 21, 2019
- Come-Together/Dinner: Feb 27, 2019 19:00-22:00
- RISC-V Activities Workshop: Feb 28, 2019 9:00-17:00

Organizing Committee

- Oliver Bringmann, Universität Tübingen, DE
- Daniel Müller-Gritschneder, Technische Universität München, DE

- Wolfgang Müller, Universität Paderborn, DE
- Jan-Hendrik Oetjens, Robert Bosch GmbH, DE
- Dieter Treytnar, edacentrum, DE
- Andreas Vörg, edacentrum, DE

Information about the organizing projects

- COMPACT website: https://www.edacentrum.de/projekte/COMPACT [17]
- CONFIRM website: https://www.edacentrum.de/projekte/CONFIRM [19]
- SAFE4I website: https://www.edacentrum.de/projekte/SAFE4I [8]

International Workshop on RISC-V Activities

Technical University Munich (TUM),Germany, 21 June 2018

The RISC-V joint academic/industry workshop aims to stimulate the exchange of information among the attendees about already existing or planned RISC-V activities. The workshop provides a platform for how these activities can be extended across projects or to develop new ideas, activities and collaborations. This workshop has been initiated by the BMBF funded projects COMPACT, CONFIRM and SAFE4I.

Deadlines

- End of registration: Jun 18, 2018
- RISC-V Workshop: Jun 21, 2018 9am - 5pm

Location: TU Munich, Arcisstr. 21, 80333 Munich, Buildung 9, 2nd floor, ROOM 4905

Workshop language: English

Registration fee: 70 € plus VAT

The program of the workshop is available at https://www.edacentrum.de/en/events/risc-v/2018/program [20] .

Organizing Committee

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- Wolfgang Müller, Universität Paderborn, DE
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Information about the organizing projects

- COMPACT website: https://www.edacentrum.de/projekte/COMPACT [17]
- CONFIRM website: https://www.edacentrum.de/projekte/CONFIRM [19]
- SAFE4I website: https://www.edacentrum.de/projekte/SAFE4I [8]

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[18] https://www.edacentrum.de/en/events/risc-v/2019/program
[19] https://www.edacentrum.de/projekte/CONFIRM
[20] https://www.edacentrum.de/en/events/risc-v/2018/program