

VLSI Reliability Aspects from a Transistor's Perspective

edaForum06 Presentation

Technical Session I

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VLSI Reliability Aspects from a Transistor

Abstract

Reliability and yield do have a severe impact on today's economic SoC manufacturing, but both still play a minor role during the entire product design stage. As device sizes shrink in future technology nodes, reliability of the used materials decreases, new reliability mechanisms occur, the complexity of the products and therefore the number of critical devices increases and last but not least the sensitivity of the circuits itself rises dramatically. Possibilities to improve product reliability at technology level are already close to their limits. Solutions on concept, architecture and circuit level are well known in principle but all of them do have quite different trade-offs with respect to area, performance and power. But how much improvement is really needed? And which solution is the most economic one? In this presentation the major reliability effects and some possible trade-offs will be discussed and required steps towards an integration into a reliability aware design process will be proposed.

Biography



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Georg Georgakos received his Diploma in electrical engineering in 1987 from the Munich University of Applied Sciences, Munich, Germany. From 1987 to 1996 he was involved in several research activities at Siemens R&D laboratories, including interconnect reliability, DUV lithography and basic analogue circuits. From 1994 until 2001 he was engaged in the development of embedded FLASH memories for automotive and smartcard applications. He started as a design engineer, took over project and program management and finally headed a group of 20 development engineers. Since 2001 he is responsible for Library Innovation within Infineon's Design Automation department. He is author and co-author of over 20 publications in international journals and conference proceedings and holds more than 15 patents.